Simple ADC is surprisingly accurate

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The reference voltage in **Fig 1a**'s simple rail-to-rail PWM ADC is the only critical component. The input-voltage range extends from ground to the power rail which also acts as the reference. The circuit is essentially a variation on the classic dual-slope integrator, the slopes being proportional to V_{IN} and $V_{REF}-V_{IN}$. The circuit works well in μP-based systems that have the spare capacity to perform the mark/space measurement and the necessary calculations.

Assuming that there is no loading, the output voltage is a square wave with amplitude equal to V_{REF} and a mean equal to V_{IN}. Provided that the period is much greater than the digital transition times, the principal source of error is the input offset voltage of the op amp. The accuracy is at least 9 bits (and more likely 12) over the full operating-input and supply-voltage range with no trims. Working with a higher supply rail yields better accuracy. You can increase resolution by lengthening the time for the mark and period.

You can also use the circuit to measure the ratio of two resistors R_U and R_L as in **Fig 1b**. The mark/space ratio is then independent of V_{REF} and equal to R_L/R_U. (DI #1443) EDN

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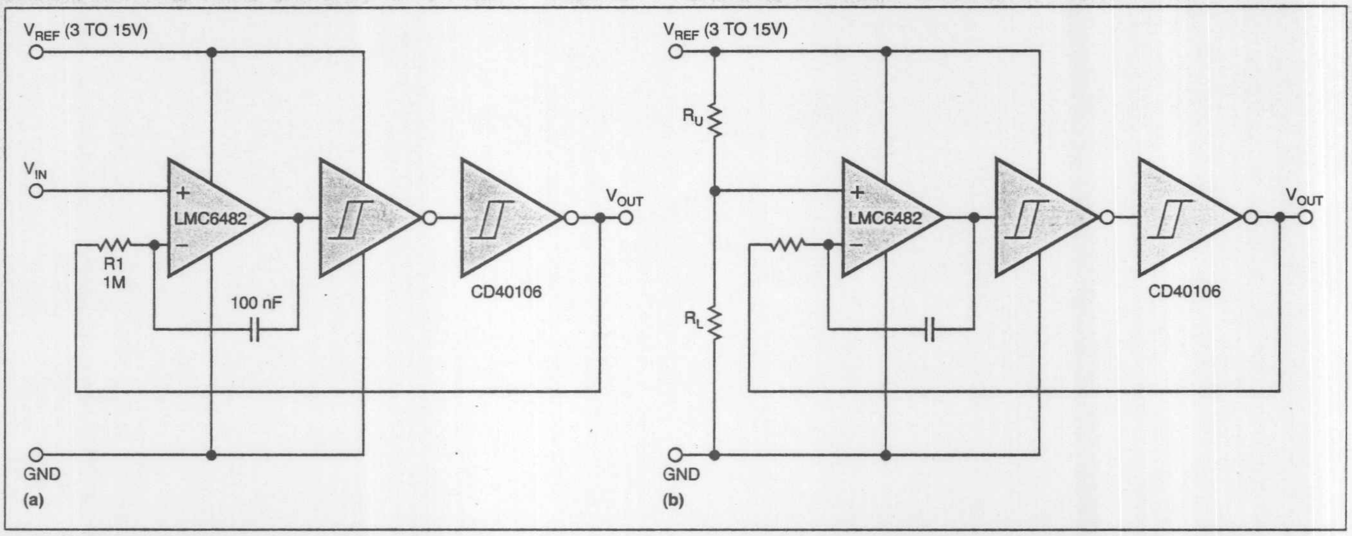

Fig 1—This simple ADC's output (a) is a PWM signal with a mark/period ratio equal to V_{REF}/V_{IN}. The circuit variation in (b) measures the ratio of R_L and R_U.

Precision clamp recovers in nanoseconds

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High-speed ADCs sometimes place very strict limits on their allowable input-voltage range, limits that generally require the use of input clamps. Some applications require very temperature-stable clamps that don't interfere with the speed of a 50-MHz amplifier. **Fig 1** shows one such circuit that clamps positive-going voltages to 1.25V at 10 mA, and you can easily adapt it for negative-going voltages and different voltage and current levels. Recovery from the clamped state occurs in about 1 nsec.

This circuit improves on the conventional diode clamp in three major areas. First, the clamping voltage drifts at only a fraction of the –2 mV/C figure of a simple diode clamp. For even lower drift, you can replace the transistors with a monolithic matched pair. Second, by using the emitter of a transistor as the clamping element, the circuit easily obtains a low clamping impedance over a very wide range of frequencies. Third, Q_1 recovers from the clamped state much faster than does a PN junction diode because there is no excess charge storage.

The op amp in the reference-circuit servo controls Q_2 to establish 1.25V at the emitter while carrying exactly 10 mA. The circuit also applies the base voltage of Q_2 to Q_1. Assuming reasonable matching of the transistors, Q_1 clamps V_{OUT} at exactly 1.25V when the clamp reaches 10 mA. This occurs when V_{IN} reaches 2V. (Transistor base currents are assumed negligible in this analysis.) The 47-pF capacitors reduce the clamping impedance of Q_1 at high frequencies.

You can easily modify the clamping voltage and current by changing V_{CLAMP} and R_{BIAS}. The circuit can clamp negative-going voltages using NPN transistors in place of Q_1 and Q_2 and changing the supply-voltage polarity. You can combine NPN- and PNP-based clamping circuits for precision clamp-